CLAIMS

1. A clock signal generator having an input at which an input clock signal is applied and having an output at which an output clock signal is provided, the clock signal generator comprising:

a synchronizing circuit having an input terminal at which the input clock signal is applied and having an output terminal at which a first clock signal is provided, the synchronizing circuit generating the first clock signal based on the input clock signal; and

a plurality of delay circuits, each having an input coupled to the output terminal of the synchronizing circuit, and having an activation terminal at which a selection signal is applied and further having an output terminal at which a respective delayed output clock signal is provided, each of the plurality of delay circuits having a respective time delay and operable to generate the respective delayed output clock signal having the respective time delay relative to the first clock signal when activated by the selection signal, one of the plurality of delay circuits activated by the selection signal to provide the respective delayed output clock signal as the output clock signal of the clock signal generator.

2. The clock signal generator of claim 1 wherein the synchronizing circuit comprises a delay-locked loop (DLL).

3. The clock signal generator of claim 2 wherein the DLL comprises a DLL having a delay component that varies proportionately as a function of input clock frequency.

4. The clock signal generator of claim 3 wherein the plurality of delay circuits comprise at least first and second delay circuits having first and second time delays, respectively, the first time delay greater than the second time delay, the first delay circuit activated for an input clock frequency less than a threshold frequency and the second delay circuit activated for an input clock frequency greater than the threshold frequency.

5. The clock signal generator of claim 1 wherein each of the plurality of delay circuits comprises a programmable delay element.

6. The clock signal generator of claim 5 wherein each of the programmable delay elements comprise a delay element programmable by programming antifuses.

7. The clock signal generator of claim 1 wherein the plurality of delay circuits are further coupled to receive as the selection signal a signal indicative of a CAS latency value.

8. The clock signal generator of claim 7 wherein the plurality of delay circuits comprise a number of delay circuits equal to the number of potential CAS latency values.

9. A clock signal generator, comprising:

a synchronizing circuit having an input terminal at which an input clock signal is applied and having an output terminal at which a first delayed clock signal is provided; and

a delay circuit having an input coupled to the output of the synchronizing circuit, an output at which an output clock signal is provided, and a selection terminal for receiving a selection signal, the delay circuit operable to provide an output clock signal having a delay with respect to the first delayed clock signal according to one of a plurality of programmable time delays selected in accordance with the selection signal.

10. The clock signal generator of claim 9 wherein the synchronizing circuit comprises a delay-locked loop (DLL).

11. The clock signal generator of claim 10 wherein the DLL comprises a DLL having a delay component that varies proportionately as a function of input clock frequency.

12. The clock signal generator of claim 11 wherein the plurality of delay circuits comprise at least first and second delay circuits having first and second time delays, respectively, the first time delay greater than the second time delay, the first delay circuit activated for an input clock frequency less than a threshold frequency and the second delay circuit activated for an input clock frequency greater than the threshold frequency.

13. The clock signal generator of claim 9 wherein each of the plurality of delay circuits comprises a programmable delay element.

14. The clock signal generator of claim 13 wherein each of the programmable delay elements comprise a delay element programmable by programming antifuses.

15. The clock signal generator of claim 9 wherein the plurality of delay circuits are further coupled to receive as the selection signal a signal indicative of a CAS latency value.

16. The clock signal generator of claim 15 wherein the plurality of delay circuits comprise a number of delay circuits equal to the number of potential CAS latency values.

17. A synchronous data output circuit, comprising:

an output driver having a data input terminal at which input data is applied, an output terminal at which output data is provided, and a clock terminal at which a clock signal is applied, the output driver operable to provide the input data as the output data in response to the clock signal;

a synchronizing circuit having an input terminal at which an external clock signal is applied and having an output terminal at which an internal clock signal is provided, the synchronizing circuit generating the internal clock signal based on the external clock signal; and

a plurality of delay circuits, each having an input coupled to the output terminal of the synchronizing circuit, and having an activation terminal to which a selection signal is applied and further having an output terminal coupled to the clock terminal of the output driver, each of the plurality of delay circuits having a respective time delay and operable to generate a respective delayed output clock signal having the respective time delay relative to the internal clock signal when activated by the selection signal, one of the plurality of delay circuits activated by the selection signal to provide the respective delayed output clock signal as the clock signal synchronizing output of data by the output driver.

18. The synchronous data output circuit of claim 17 further comprising a data strobe signal generator coupled to the output driver to generate a data strobe signal, the output driver further operable to output the data strobe signal in response to the clock signal applied to the clock terminal.

19. The synchronous data output circuit of claim 17 wherein the synchronizing circuit comprises a delay-locked loop (DLL).

20. The synchronous data output circuit of claim 19 wherein the DLL comprises a DLL having a delay component that varies proportionately as a function of input clock frequency and wherein the plurality of delay circuits comprise at least first and second delay circuits having first and second time delays, respectively, the first time delay greater than the second time delay, the first delay circuit activated for an input clock frequency less than a threshold frequency and the second delay circuit activated for an input clock frequency greater than the threshold frequency.

21. The synchronous data output circuit of claim 17 wherein each of the plurality of delay circuits comprises a programmable delay element having programmable time delays set by programming antifuses.

22. The synchronous data output circuit of claim 17 wherein the plurality of delay circuits are further coupled to receive as the selection signal a signal indicative of a CAS latency value and the plurality of delay circuits comprise a number of delay circuits equal to the number of potential CAS latency values.

23. A memory device, comprising:

an address bus;

a control bus;

an internal data bus;

an address decoder coupled to the address bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit; and

a read/write circuit coupled to the memory-cell array through the internal data bus to output data received from the memory-cell array, the read/write circuit including a synchronous data output circuit, comprising:

an output driver having a data input terminal coupled to the internal data bus to receive input data, an output terminal at which output data is provided, and a clock terminal at which a clock signal is applied, the output driver operable to provide the input data as the output data in response to the clock signal;

a synchronizing circuit having an input terminal at which an external clock signal is applied and having an output terminal at which an internal clock signal is provided, the synchronizing circuit generating the internal clock signal based on the external clock signal; and

a plurality of delay circuits, each having an input coupled to the output terminal of the synchronizing circuit, and having an activation terminal to which a selection signal is applied and further having an output terminal coupled to the clock terminal of the output driver, each of the plurality of delay circuits having a respective time delay and operable to generate a respective delayed output clock signal having the respective time delay relative to the internal clock signal when activated by the selection signal, one of the plurality of delay circuits

activated by the selection signal to provide the respective delayed output clock signal as the clock signal synchronizing output of data by the output driver.

24. The memory device of claim 23 wherein the synchronous data output circuit further comprises a data strobe signal generator coupled to the output driver to generate a data strobe signal, the output driver further operable to output the data strobe signal in response to the clock signal applied to the clock terminal.

25. The memory device of claim 23 wherein the synchronizing circuit of the synchronous data output circuit comprises a delay-locked loop (DLL).

26. The memory device of claim 25 wherein the DLL comprises a DLL having a delay component that varies proportionately as a function of input clock frequency.

27. The memory device of claim 26 wherein the plurality of delay circuits comprise at least first and second delay circuits having first and second time delays, respectively, the first time delay greater than the second time delay, the first delay circuit activated for an input clock frequency less than a threshold frequency and the second delay circuit activated for an input clock frequency greater than the threshold frequency.

28. The memory device of claim 23 wherein each of the plurality of delay circuits comprises a programmable delay element.

29. The memory device of claim 28 wherein each of the programmable delay elements comprise a delay element programmable by programming antifuses.

30. The memory device of claim 23 wherein the plurality of delay circuits are further coupled to receive as the selection signal a signal indicative of a CAS latency value.

31. The memory device of claim 30 wherein the plurality of delay circuits comprise a number of delay circuits equal to the number of potential CAS latency values.

32. A memory device, comprising:

an address bus;

a control bus;

an internal data bus;

an address decoder coupled to the address bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit; and

a read/write circuit coupled to the memory-cell array through the internal data bus to output data received from the memory-cell array, the read/write circuit including a synchronous data output circuit, comprising:

an output driver having a data input terminal coupled to the internal data bus to receive input data, an output terminal at which output data is provided, and a clock terminal at which a clock signal is applied, the output driver operable to provide the input data as the output data in response to the clock signal;

a synchronizing circuit having an input terminal at which an external clock signal is applied and having an output terminal at which an internal clock signal is provided; and

a delay circuit having an input coupled to the output of the synchronizing circuit, an output coupled to the clock terminal of the output driver, and a selection terminal for receiving a selection signal, the delay circuit operable to provide the clock signal to synchronize output by the output driver having a delay with respect to the internal clock signal according to one of a plurality of programmable time delays selected in accordance with the selection signal.

33. The memory device of claim 32 wherein the synchronous data output circuit further comprises a data strobe signal generator coupled to the output driver to generate a

data strobe signal, the output driver further operable to output the data strobe signal in response to the clock signal applied to the clock terminal.

34. The memory device of claim 32 wherein the synchronizing circuit of the synchronous data output circuit comprises a delay-locked loop (DLL).

35. The memory device of claim 34 wherein the DLL comprises a DLL having a delay component that varies proportionately as a function of input clock frequency.

36. The memory device of claim 35 wherein the plurality of delay circuits comprise at least first and second delay circuits having first and second time delays, respectively, the first time delay greater than the second time delay, the first delay circuit activated for an input clock frequency less than a threshold frequency and the second delay circuit activated for an input clock frequency greater than the threshold frequency.

37. The memory device of claim 32 wherein each of the plurality of delay circuits comprises a programmable delay element.

38. The memory device of claim 37 wherein each of the programmable delay elements comprise a delay element programmable by programming antifuses.

39. The memory device of claim 32 wherein the plurality of delay circuits are further coupled to receive as the selection signal a signal indicative of a CAS latency value.

40. The memory device of claim 39 wherein the plurality of delay circuits comprise a number of delay circuits equal to the number of potential CAS latency values.

41. A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a memory device coupled to the processor, the memory device, comprising:

an address bus;

a control bus;

an internal data bus;

an address decoder coupled to the address bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit; and

a read/write circuit coupled to the memory-cell array through the internal data bus to output data received from the memory-cell array, the read/write circuit including a synchronous data output circuit, comprising:

an output driver having a data input terminal coupled to the internal data bus to receive input data, an output terminal at which output data is provided, and a clock terminal at which a clock signal is applied, the output driver operable to provide the input data as the output data in response to the clock signal;

a synchronizing circuit having an input terminal at which an external clock signal is applied and having an output terminal at which an internal clock signal is provided; and

a delay circuit having an input coupled to the output of the synchronizing circuit, an output coupled to the clock terminal of the output driver, and a selection terminal for receiving a selection signal, the delay circuit operable to provide the clock signal to synchronize output by the output driver having a delay with respect to the internal clock signal according to one of a plurality of programmable time delays selected in accordance with the selection signal.

42. The computer system of claim 41 wherein the synchronous data output circuit further comprises a data strobe signal generator coupled to the output driver to generate a data strobe signal, the output driver further operable to output the data strobe signal in response to the clock signal applied to the clock terminal.

43. The computer system of claim 41 wherein the synchronizing circuit of the synchronous data output circuit comprises a delay-locked loop (DLL).

44. The computer system of claim 43 wherein the DLL comprises a DLL having a delay component that varies proportionately as a function of input clock frequency.

45. The computer system of claim 44 wherein the plurality of delay circuits comprise at least first and second delay circuits having first and second time delays, respectively, the first time delay greater than the second time delay, the first delay circuit activated for an input clock frequency less than a threshold frequency and the second delay circuit activated for an input clock frequency greater than the threshold frequency.

46. The computer system of claim 41 wherein each of the plurality of delay circuits comprises a programmable delay element.

47. The computer system of claim 46 wherein each of the programmable delay elements comprise a delay element programmable by programming antifuses.

48. The computer system of claim 41 wherein the plurality of delay circuits are further coupled to receive as the selection signal a signal indicative of a CAS latency value.

49. The computer system of claim 48 wherein the plurality of delay circuits comprise a number of delay circuits equal to the number of potential CAS latency values.

50. A method of generating a clock signal, comprising:

synchronizing an internal clock signal to an external clock signal; and

delaying the internal clock signal different amounts based on a selection value indicative of external clock frequency to provide the clock signal.

51. The method of claim 50 wherein delaying the internal clock signal different amounts based on a selection value comprises delaying the internal clock signal different amounts based on a CAS latency value.

52. The method of claim 50 wherein delaying the internal clock signal different amounts based on a selection value comprises activating one of a plurality of delay circuits coupled to receive the internal clock signal and having a respective time delay, the activated delay circuit providing an output clock signal having the respective delay relative to the internal clock signal for use as the clock signal.

53. The method of claim 52 wherein delaying the internal clock signal different amounts based on a selection value comprises selecting one of the plurality of delay circuits to activate based on a CAS latency value.

54. The method of claim 53 wherein the plurality of delay circuits comprises a number of delay circuits equal to the number of possible CAS latency values.